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Substitute for form 1449/PTO				<b>Complete if Known</b>	
<b>FIFTH SUPPLEMENTAL                  INFORMATION DISCLOSURE                  STATEMENT BY APPLICANT</b> <i>(Use as many sheets as necessary)</i>				Application Number	10/060,086
				Filing Date	January 31, 2002
				First Named Inventor	Sanjiv GARG
				Art Unit	2154
				Examiner Name	Larry D. Donaghue
Sheet	1	of	1	Attorney Docket Number	2047.0600007

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code <sup>2</sup> (if Known)			
/LD/	US1	5,179,689	01-12-1993	Leach <i>et al.</i>	
/LD/	US2	5,249,286	09-28-1993	Alpert <i>et al.</i>	
/LD/	US3	4,980,817	12-25-1990	Fossum <i>et al.</i>	
	US4				
	US5				
	US6				
	US7				
	US8				
	US9				
	US10				
	US11				
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	US13				
	US14				
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FOREIGN PATENT DOCUMENTS						
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		Country Code <sup>3</sup> Number <sup>4</sup> Kind Code <sup>5</sup> (if known)				
	FP1					
	FP2					
	FP3					
	FP4					
	FP5					
	FP6					
	FP7					
	FP8					
	FP9					

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NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T <sup>2</sup>
/LD/	NPL1	<i>Complaint</i> , 7 pages, filed October 11, 2006, in Transmeta Corporation v. Intel Corporation, in the U.S. District Court for the District of Delaware, Case No. 1:06-cv-00633.	
/LD/	NPL2	<i>First Amended Complaint</i> , 7 pages, filed December 12, 2006, in Transmeta Corporation v. Intel Corporation, in the U.S. District Court for the District of Delaware, Case No. 1:06-cv-00633.	
/LD/	NPL3	<i>Intel Corporation's Answer, Affirmative Defenses, and Counterclaims to Transmeta's First Amended Complaint</i> , 27 pages, filed January 9, 2007, in Transmeta Corporation v. Intel Corporation, in the U.S. District Court for the District of Delaware, Case No. 1:06-cv-00633.	
/LD/	NPL4	G. Myers <i>et al.</i> , <i>The 80960 Microprocessor Architecture</i> , John Wiley & Sons, Inc., 1988.	
/LD/	NPL5	<i>Third-Generation TMS320 User's Guide</i> , Texas Instruments, 1988.	
/LD/	NPL6	<i>Convex Architecture Handbook, Version 1</i> , Convex Computer Corporation, 1984.	
/LD/	NPL7	Butler, M. <i>et al.</i> , "Single Instruction Stream Parallelism Is Greater than Two," <i>Proceedings of the 18th Annual International Symposium on Computer Architecture</i> , ACM, pp. 276-286 (May 1991).	
/LD/	NPL8	Hennessy, J.L. and Patterson, D.A., <i>Computer Architecture: A Quantitative Approach</i> , Morgan Kaufmann Publishers, pp. xi-xv, 257-278, 290-314 and 449 (1990).	
/LD/	NPL9	Peleg, A. and Weiser, U., "Future Trends in Microprocessors: Out-of-Order Execution, Speculative Branching and their CISC Performance Potential", IEEE, pp. 263-266 (1991).	
/LD/	NPL10	Swensen, J.A. and Patt, Y.N., "Hierarchical Registers for Scientific Computers," <i>Conference Proceedings: 1988 International Conference on Supercomputing</i> , ICS, July 4-8, 1988, pp. 346-353.	

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/LD/	NPL11	Butler, M. and Patt, Y., "An Improved Area-Efficient Register Alias Table for Implementing HPS," University of Michigan, Ann Arbor, Michigan, 24 pages (January 1990).	
/LD/	NPL12	Hwu, W. and Patt, Y., "Design Choices for the HPSm Microprocessor Chip," <i>Proceedings of the Twentieth Annual Hawaii International Conference on System Sciences</i> , pp. 330-336 (1987).	
/LD/	NPL13	Hwu, W-M. et al., "An HPS Implementation of VAX: Initial Design and Analysis," <i>Proceedings of the Nineteenth Annual Hawaii International Conference on System Sciences</i> , pp. 282-291 (1986).	
/LD/	NPL14	Hwu, W. and Patt, Y., "HPSm2: A Refined Single-Chip Microengine," <i>HICSS '88</i> , IEEE, pp. 30-40 (1988).	
/LD/	NPL15	Patt, Y.N. et al., "Experiments with HPS, a Restricted Data Flow Microarchitecture for High Performance Computers," <i>COMPCON 86</i> , IEEE, pp. 254-258 (1986).	
/LD/	NPL16	Patt et al., "Run-Time Generation of HPS Microinstructions From a VAX Instruction Stream," <i>Proceedings of MICRO 19 Workshop</i> , New York, pp. 75-81 (October 1986).	
/LD/	NPL17	Wilson, J.E. et al., "On Tuning the Microarchitecture of an HPS Implementation of the VAX," <i>Proceedings of the 20th Annual Workshop on Microprogramming</i> , IEEE Computer Society, pp. 162-167 (December 1-4, 1987).	
	NPL18		
	NPL19		
	NPL20		

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